ABSTRACT OF THE DISCLOSURE

A starvation avoidance mechanism for an input/output node of a computer system. A scheduler unit includes a first buffer circuit and a second buffer circuit. The first buffer circuit includes a first plurality of buffers for storing selected control commands received from a first source and the second buffer circuit includes a second plurality of buffers for storing selected control commands received from a second source. The scheduler further includes an arbitration circuit coupled to the first buffer circuit and to the second buffer circuit. The arbitration circuit may be configured to arbitrate between the control commands stored in the first buffer circuit and the control commands stored in the second buffer circuit. The outcome of selected arbitration cycles may be dependent upon a number of times in which a control command from a given one of the buffers is blocked due to an unavailable destination.